ABSTRACT

A method for securing port bypass circuit settings is presented comprising issuing one or more command(s) to one or more inputs of a general purpose input/output (GPIO) system, wherein the command(s) cause a first output of the GPIO system associated with a first input of the multiple inputs to issue a control signal to a latch associated with a port bypass circuit (PBC) addressed in the received command(s), and a second output of the GPIO system associated with a second of the multiple inputs of the GPIO system to issue a clock signal to a latch associated a PBC addressed in the received command(s). If command(s) received at the first and second inputs are consistent with changing the state of a common PBC, the control signal and the clock signal are sent to a single latching device, which latches the control signal to the addressed PBC changing the state of the PBC. If the command(s) are not consistent, the control and clock signal(s) are not received by a common latch, and the PBC states remain unchanged.